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1 **Diagnosis and repair of memory with coupling faults**
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31 **An approach for online repair and yield enhancement of VLSI/WSI redundant memories**
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CompEuro '91. 'Advanced Computer Technology, Reliable Systems and Applications'. 5th Annual European Computer Conference. Proceedings. , 13-1 May 1991
Pages:685 - 689

[Abstract] [PDF Full-Text (404 KB)] **IEEE CNF**

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32 **Wafer scale integration (WSI) of programmable gate arrays (PGA's**
McDonald, J.F.; Dabral, S.; Philhower, R.; Russinovich, M.E.;
Wafer Scale Integration, 1990. Proceedings., [2nd] International Conference on , 23-25 Jan. 1990
Pages:329 - 338

[Abstract] [PDF Full-Text (588 KB)] **IEEE CNF**

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33 **A 50 ns 16 Mb DRAM with a 10 ns data rate**
Kalter, H.; Barth, J.; Dilorenzo, J.; Drake, C.; Fifield, J.; Hovis, W.; Kelley, G., Lewis, S.; Nickel, J.; Stapper, C.; Yankosky, J.;
Solid-State Circuits Conference, 1990. Digest of Technical Papers. 37th ISSCC 1990 IEEE International , 14-16 Feb. 1990
Pages:232 - 233, 303

[Abstract] [PDF Full-Text (720 KB)] **IEEE CNF**

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34 **Approaches for the repair of VLSI/WSI RRAMs by row/column dele**
Lombardi, F.; Huang, W.K.;
Fault-Tolerant Computing, 1988. FTCS-18, Digest of Papers., Eighteenth

International Symposium on , 27-30 June 1988
Pages:342 - 347

[Abstract] [PDF Full-Text (444 KB)] **IEEE CNF**

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<sentence> column) <and>
((second <phrase> pass)
<sentence> row)
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(self <phrase> test)) <and>
((first <phrase> pass)
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(self <phrase> test))
<phrase> (method <or> process
<or> procedure)) <and>
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Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC 1992 IEEE International , 19-21 Feb. 1992
Pages:216 - 217, 288

[Abstract] [PDF Full-Text (204 KB)] **IEEE CNF**

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2 **Built in self repair for embedded high density SRAM**
Ilyoung Kim; Zorian, Y.; Komoriya, G.; Pham, H.; Higgins, F.P.; Lewandowski,
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
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memory) <and> ((bist <or>
self-test <or> (self <phrase>
test)) <phrase> (method <or>
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((bist <or> self-test <or>
(self <phrase> test))
<phrase> (method <or> process
<or> procedure)) <and>
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test <or> (self <phrase>
test)) <and> ((redundant <or>
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1 **SRAM embedded memory with low cost, flash EEPROM-switch-contr redundancy**
McPartland, R.J.; Loeper, D.J.; Higgins, F.P.; Singh, R.; MacDonald, G.; Komo G.; Aymeloglu, S.; DePaolis, M.V.; Leung, C.W.;
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1 **A new column redundancy scheme for fast access time of 64-Mb DR**
Jun, Y.-H.; Jeong, W.-H.; Park, J.-H.; Kim, T.-H.; Kim, S.-W.; Lee, J.-S.; Jang J.; Khang, C.-M.; Lee, H.-G.;
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on , 3-6 May 1993
Pages:1937 - 1940 vol.3

[Abstract] [PDF Full-Text (264 KB)] **IEEE CNF**

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2 **A 1.6-GByte/s DRAM with flexible mapping redundancy technique a additional refresh scheme**
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Pages:940 - 942

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5 **0.13-µm 32-Mb/64-Mb embedded DRAM core with high efficient redundancy and enhanced testability**
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Pages:705 - 712

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Pages:287 - 289

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10 **Integration of SRAM redundancy into production test**
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Pages:187 - 193

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11 **Dynamically shift-switched dataline redundancy suitable for DRAM macro with wide data bus**
Namekawa, T.; Miyano, S.; Fukuda, R.; Haga, R.; Wada, O.; Banba, H.; Take S.; Suda, K.; Mimoto, K.; Yamaguchi, S.; Ohkubo, T.; Takato, H.; Numata, K.
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[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

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[Abstract] [PDF Full-Text (500 KB)] **IEEE CNF**

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On-Line Testing Workshop, 2000. Proceedings. 6th IEEE International , 3-5 Ju 2000
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